

16 Mbit (1M x 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V to 2.25 V
- Ultra low standby power
 - Typical standby current: 1.5 μ A
 - Maximum standby current: 12 μ A
- Ultra low active power
 - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball very fine ball grid array (VFBGA) packages

Functional Description

The CY62167EV18 is a high performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption

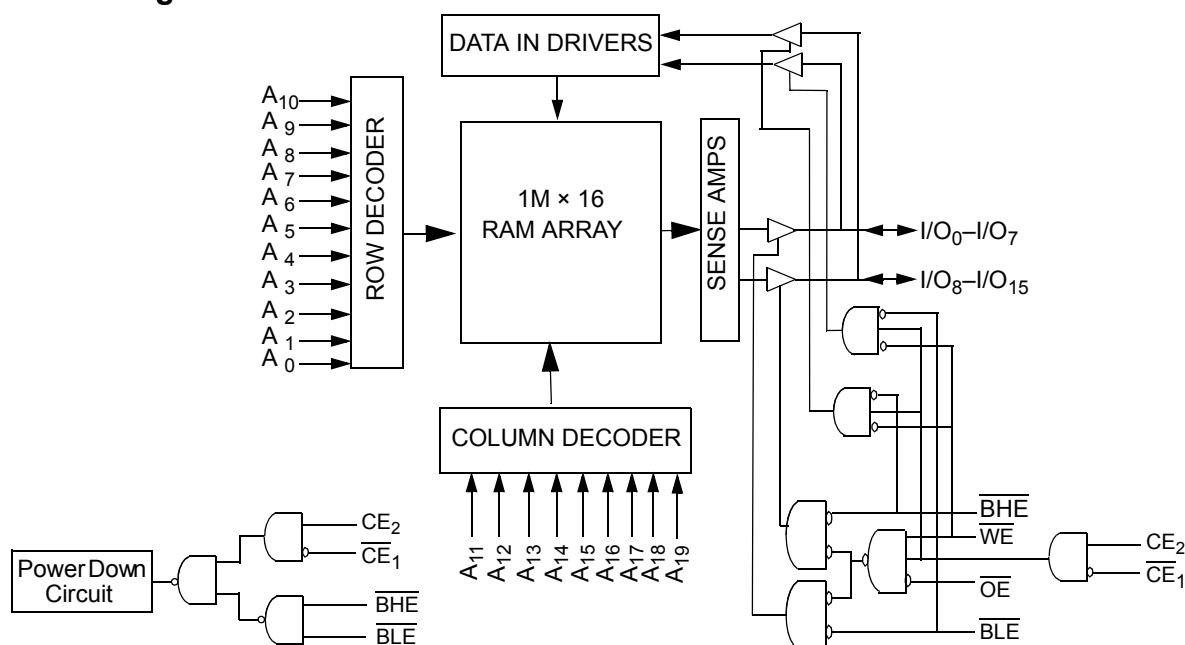
by 99 percent when addresses are not toggling. Place the device into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when: the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW); outputs are disabled (\overline{OE} HIGH); both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH); and a write operation is in progress (CE_1 LOW, CE_2 HIGH and WE LOW).

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the [Truth Table on page 10](#) for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Logic Block Diagram

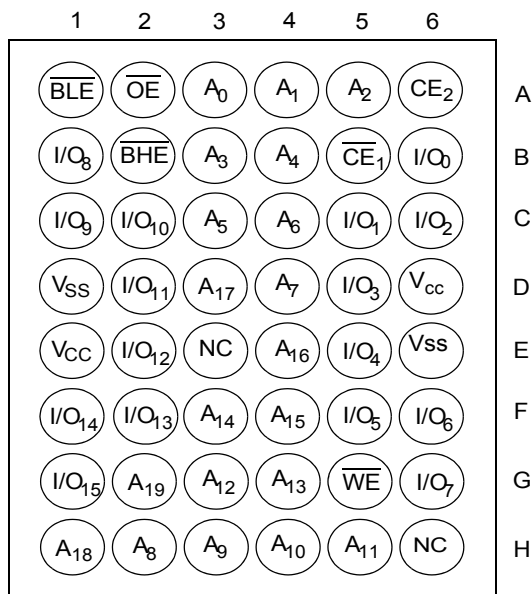


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Pin Configuration

Figure 1. 48-Ball VFBGA (6 × 8 × 1 mm) Top View [1, 2]



Product Portfolio

| Product | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|------------------------------|---------------------------|--------------------|------|------------|--------------------------------|-----|----------------------|-----|-------------------------------|-----|
| | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | | | | f = 1 MHz | | f = f _{max} | | | |
| | Min | Typ ^[3] | Max | | Typ ^[3] | Max | Typ ^[3] | Max | Typ ^[3] | Max |
| CY62167EV18LL | 1.65 | 1.8 | 2.25 | 55 | 2.2 | 4.0 | 25 | 30 | 1.5 | 12 |
| CY62167EV30LL ^[4] | | | | | | | | | | |

Notes

1. NC pins are not connected on the die.
2. Ball H6 for the VFBGA package can be used to upgrade to a 32 M density.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
4. This part can be operated in the V_{CC} range of 1.65 V–2.25 V at 55ns speed. It can also be operated in the V_{CC} range of 2.2 V–3.6 V at 45ns speed.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.2 V to 2.45 V ($V_{CC}(\text{max}) + 0.2 \text{ V}$)

DC voltage applied to outputs in High Z state^[5, 6] -0.2 V to 2.45 V ($V_{CC}(\text{max}) + 0.2 \text{ V}$)

DC input voltage^[5, 6] -0.2 V to 2.45 V ($V_{CC}(\text{max}) + 0.2 \text{ V}$)

Output current into outputs (LOW) 20 mA

Static discharge voltage >2001 V (MIL-STD-883, Method 3015)

Latch up current >200 mA

Operating Range

| Device | Range | Ambient Temperature | $V_{CC}^{[7]}$ |
|---------------|------------|---------------------|------------------|
| CY62167EV18LL | Industrial | -40 °C to +85 °C | 1.65 V to 2.25 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 55 ns | | | Unit |
|-----------------|--|--|-------|--------------------|--------------------------|------|
| | | | Min | Typ ^[8] | Max | |
| V_{OH} | Output HIGH voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.4 | — | — | V |
| V_{OL} | Output LOW voltage | $I_{OL} = 0.1 \text{ mA}$ | — | — | 0.2 | V |
| V_{IH} | Input HIGH voltage | $V_{CC} = 1.65 \text{ V to } 2.25 \text{ V}$ | 1.4 | — | $V_{CC} + 0.2 \text{ V}$ | V |
| V_{IL} | Input LOW voltage | $V_{CC} = 1.65 \text{ V to } 2.25 \text{ V}$ | -0.2 | — | 0.4 | V |
| I_{IX} | Input leakage current | $GND \leq V_I \leq V_{CC}$ | -1 | — | +1 | μA |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -1 | — | +1 | μA |
| I_{CC} | V_{CC} operating supply current | $f = f_{\text{max}} = 1/t_{RC}$ $V_{CC} = V_{CC}(\text{max})$ | — | 25 | 30 | mA |
| | | $f = 1 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ CMOS levels | — | 2.2 | 4.0 | |
| I_{SB1} | Automatic power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$ $f = f_{\text{max}}$ (address and data only), $f = 0$ (OE, and WE), $V_{CC} = V_{CC}(\text{max})$ | — | 1.5 | 12 | μA |
| $I_{SB2}^{[9]}$ | Automatic power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC}(\text{max})$ | — | 1.5 | 12 | μA |

Capacitance

| Parameter ^[10] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C_{IN} | Input capacitance | $T_A = 25 \text{ °C}$, $f = 1 \text{ MHz}$, | 10 | pF |
| C_{OUT} | Output capacitance | $V_{CC} = V_{CC}(\text{typ})$ | 10 | pF |

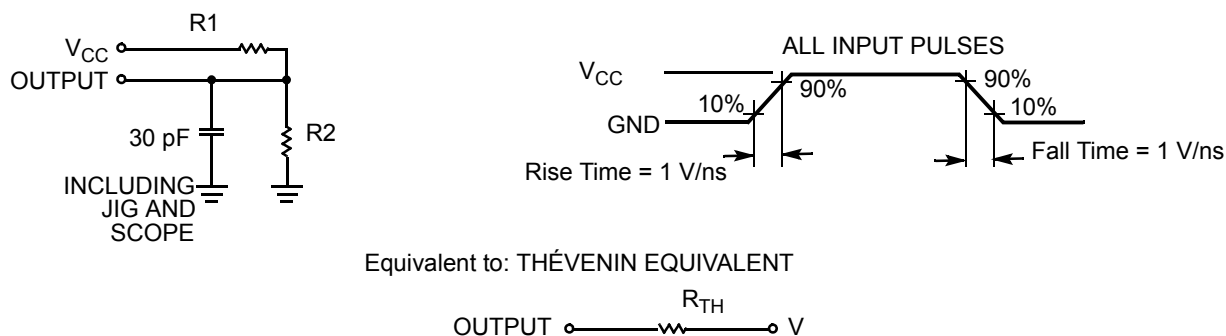
Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$ for pulse durations less than 20 ns.
- $V_{IH}(\text{max}) = V_{CC} + 0.75 \text{ V}$ for pulse durations less than 20 ns.
- Full Device AC operation is based on a 100 μs ramp time from 0 to $V_{CC}(\text{min})$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(\text{typ})$, $T_A = 25 \text{ °C}$.
- Chip enables (\overline{CE}_1 and CE_2), and byte enables (\overline{BHE} and \overline{BLE}) must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

| Parameter ^[11] | Description | Test Conditions | VFBGA (6 × 8 × 1mm) | Unit |
|---------------------------|---|---|------------------------|------|
| Θ_{JA} | Thermal resistance (Junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 55 | °C/W |
| Θ_{JC} | Thermal resistance (Junction to case) | | 16 | °C/W |

Figure 2. AC Test Loads and Waveforms



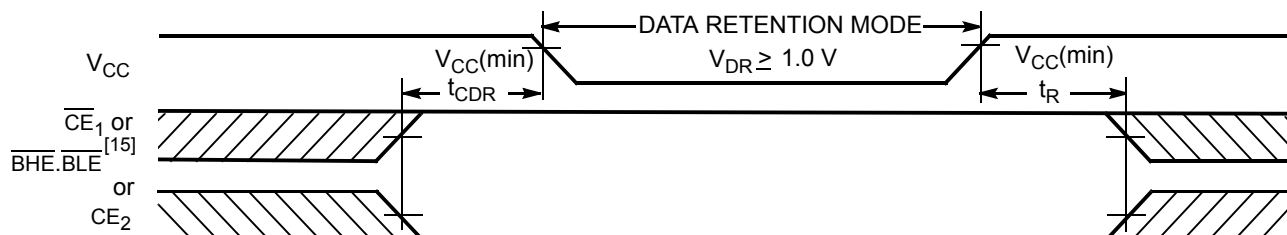
| Parameters | 1.8 V | Unit |
|-----------------|-------|------|
| R1 | 13500 | Ω |
| R2 | 10800 | Ω |
| R _{TH} | 6000 | Ω |
| V _{TH} | 0.80 | V |

Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[12] | Max | Unit |
|-----------------------------------|--------------------------------------|---|-----|---------------------|-----|------|
| V _{DR} | V _{CC} for data retention | | 1.0 | – | – | V |
| I _{CCDR} ^[13] | Data retention current | V _{CC} = 1.0 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and \overline{BLE}) $\geq V_{CC} - 0.2$ V, V _{IN} $\geq V_{CC} - 0.2$ V or V _{IN} ≤ 0.2 V | – | – | 10 | μA |
| t _{CDR} ^[11] | Chip deselect to data retention time | | 0 | – | – | ns |
| t _R ^[14] | Operation recovery time | | 55 | – | – | ns |

Figure 3. Data Retention Waveform



Notes

11. Tested initially and after any design or process changes that may affect these parameters.
12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
13. Chip enables (CE₁ and CE₂), and byte enables (BHE and BLE) must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
15. BHE, BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

| Parameter ^[16, 17] | Description | 55 ns | | Unit |
|-------------------------------|--|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t _{RC} | Read cycle time | 55 | – | ns |
| t _{AA} | Address to data valid | – | 55 | ns |
| t _{OHA} | Data hold from address change | 10 | – | ns |
| t _{ACE} | \overline{CE}_1 LOW and CE ₂ HIGH to data valid | – | 55 | ns |
| t _{DOE} | \overline{OE} LOW to data valid | – | 25 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[18] | 5 | – | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[18, 19] | – | 18 | ns |
| t _{LZCE} | \overline{CE}_1 LOW and CE ₂ HIGH to Low Z ^[18] | 10 | – | ns |
| t _{HZCE} | \overline{CE}_1 HIGH and CE ₂ LOW to High Z ^[18, 19] | – | 18 | ns |
| t _{PU} | \overline{CE}_1 LOW and CE ₂ HIGH to power-up | 0 | – | ns |
| t _{PD} | \overline{CE}_1 HIGH and CE ₂ LOW to Power-down | – | 55 | ns |
| t _{DBE} | BLE/BHE LOW to data valid | – | 55 | ns |
| t _{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[18] | 10 | – | ns |
| t _{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[18, 19] | – | 18 | ns |
| Write Cycle ^[20] | | | | |
| t _{WC} | Write cycle time | 55 | – | ns |
| t _{SCE} | \overline{CE}_1 LOW and CE ₂ HIGH to write end | 40 | – | ns |
| t _{AW} | Address setup to write end | 40 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | ns |
| t _{SA} | Address setup to write start | 0 | – | ns |
| t _{PWE} | \overline{WE} pulse Width | 40 | – | ns |
| t _{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 40 | – | ns |
| t _{SD} | Data setup to write end | 25 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[18, 19] | – | 20 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[18] | 10 | – | ns |

Notes

16. Test conditions for all parameters other than tri-state parameters are based on signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [AC Test Loads and Waveforms on page 5](#).
17. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See [application note AN13842](#) for further clarification.
18. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
19. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the output enters a high impedance state.
20. The internal memory write time is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, BHE and/or BLE = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled).^[21, 22]

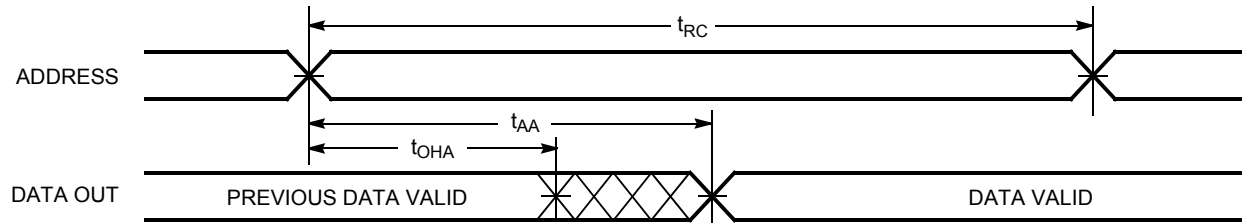
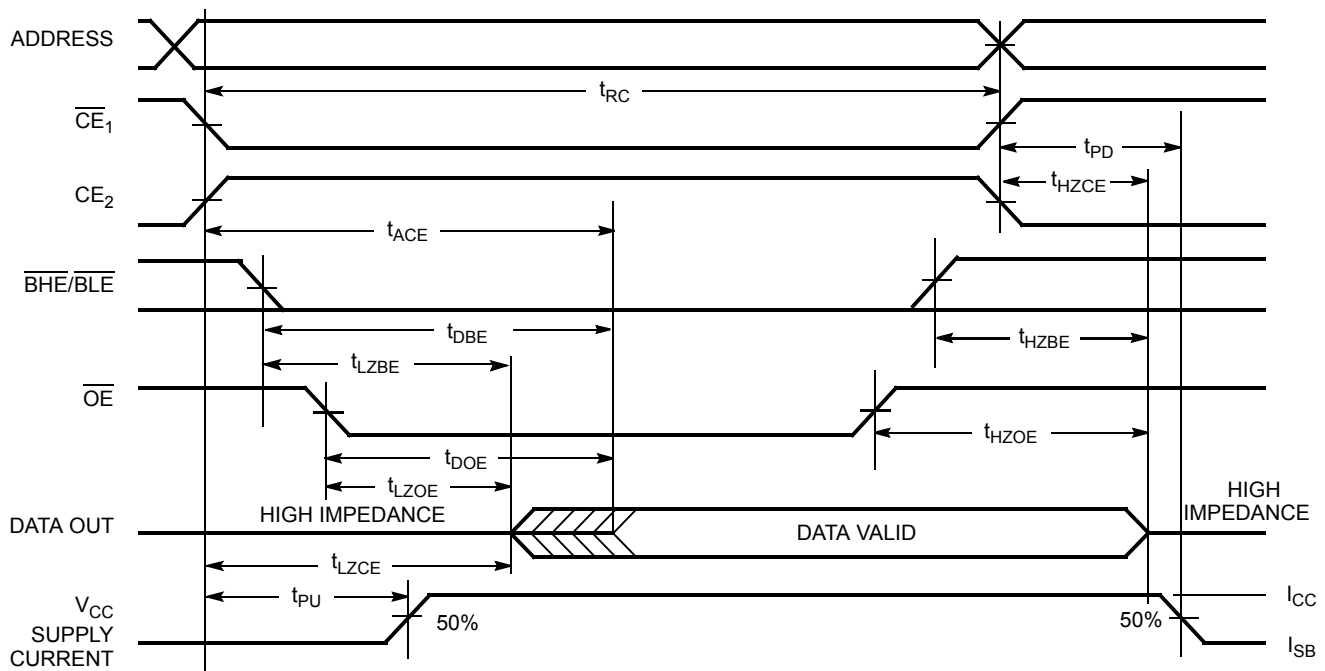
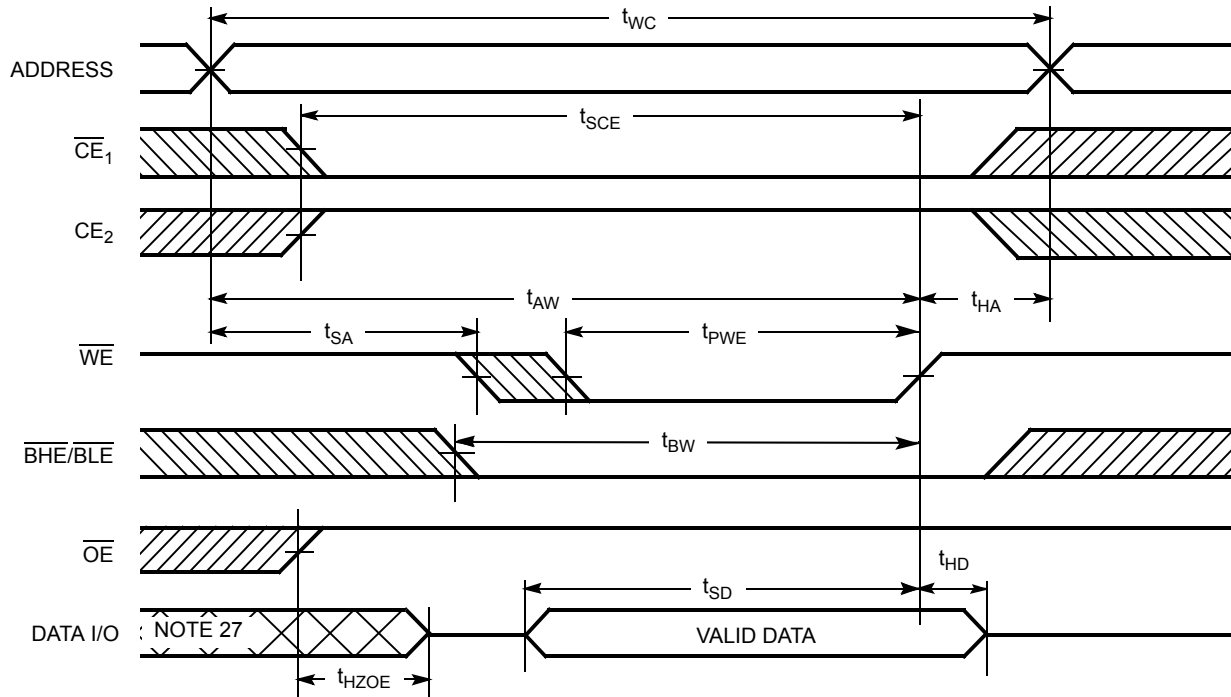
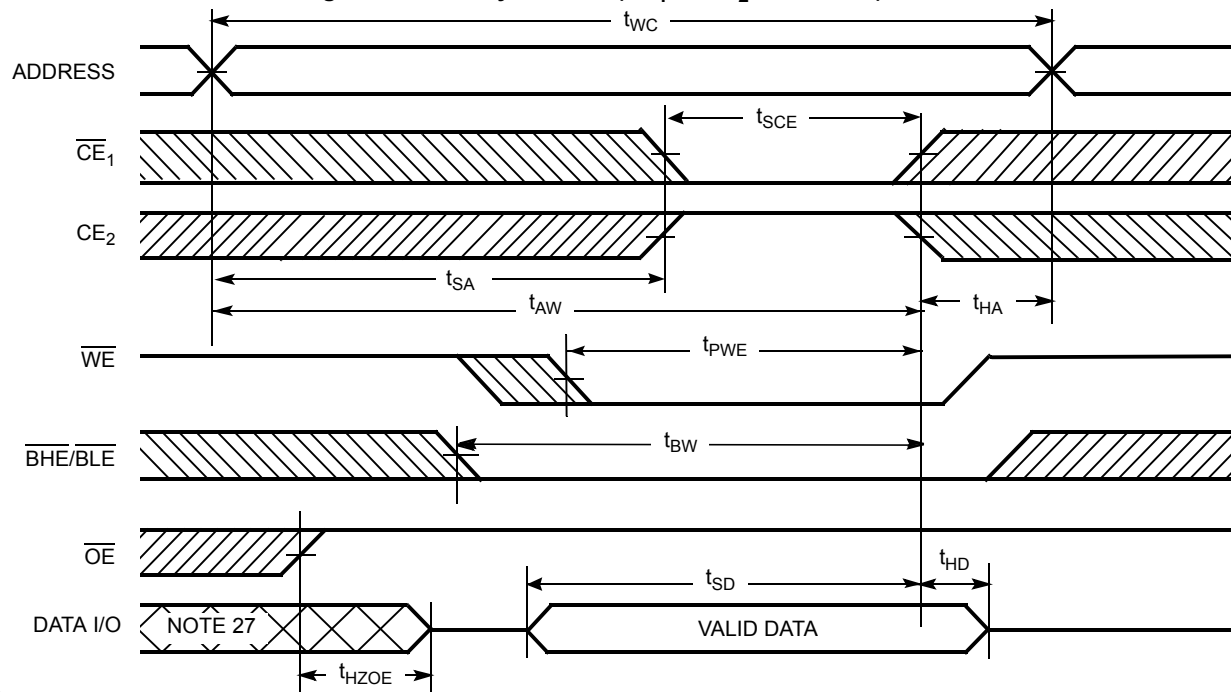


Figure 5. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[22, 23]

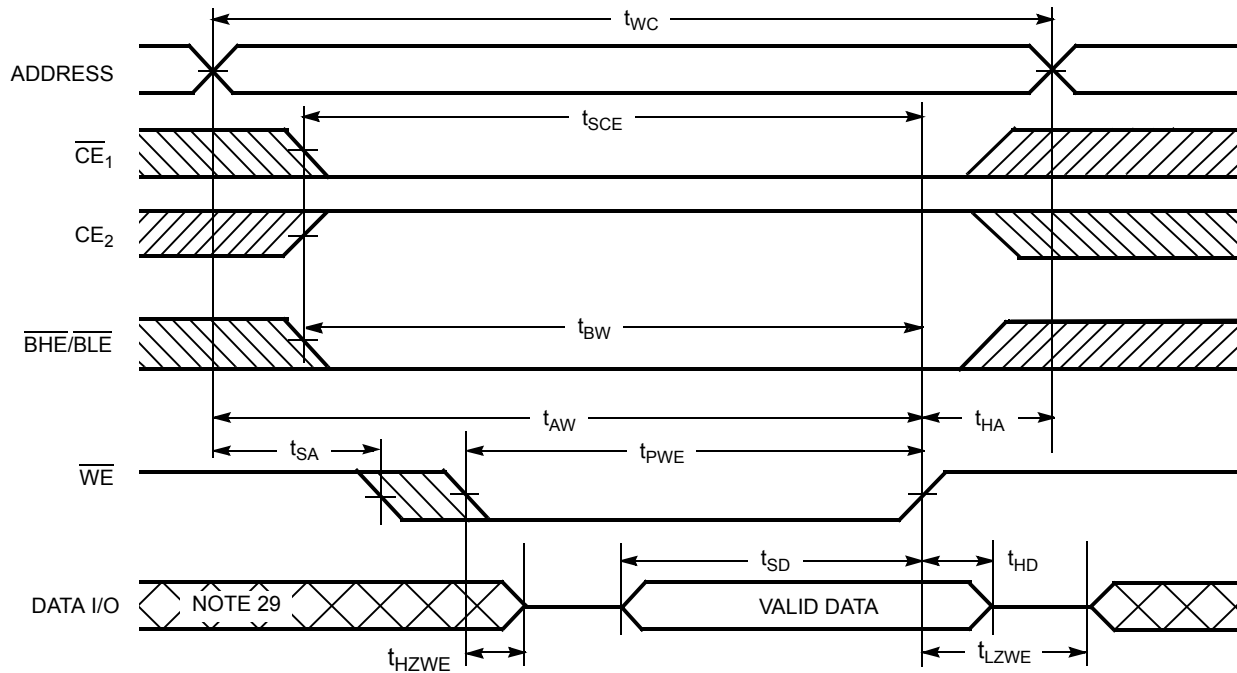
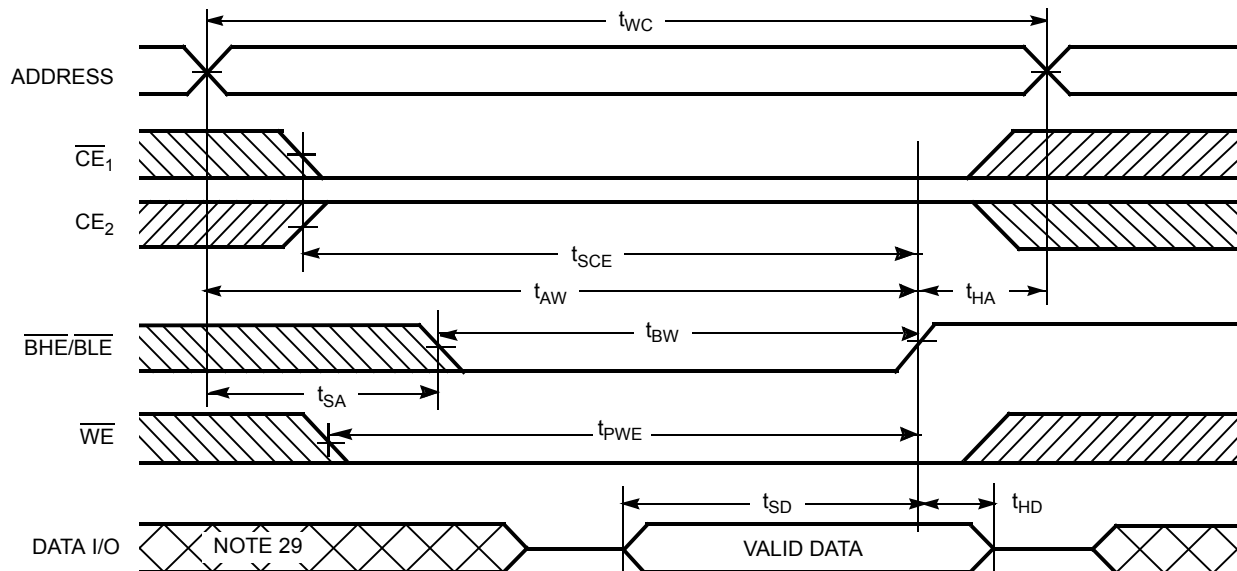


Notes

21. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$.
22. WE is HIGH for read cycle.
23. Address valid before or similar to $\overline{\text{CE}}_1$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Figure 6. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)^[24, 25, 26]

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE_2 Controlled)^[24, 25, 26]

Notes

24. The internal memory write time is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IL}$, and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\text{OE} = V_{IH}$.
26. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
27. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Figure 8. Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW)^[28]

Figure 9. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} Low)^[28]

Notes

28. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
 29. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

| \overline{CE}_1 | \overline{CE}_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X ^[30] | X | X | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| X ^[30] | L | X | X | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| X ^[30] | X ^[30] | X | X | H | H | High Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | H | L | H | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | L | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |

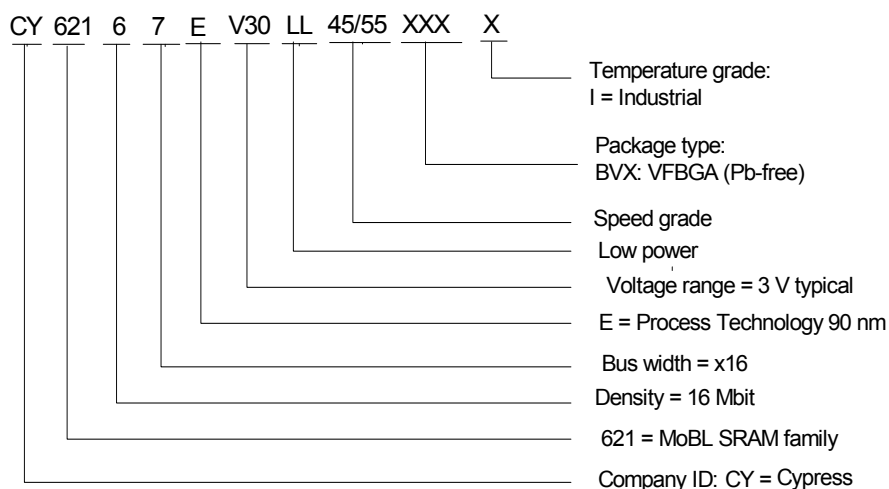
Note

30. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-------------------------------------|-----------------|--|-----------------|
| 55 | CY62167EV18LL-55BVI | 51-85150 | 48-ball VFBGA (6 × 8 × 1 mm) | Industrial |
| | CY62167EV18LL-55BVXI | | 48-ball VFBGA (6 × 8 × 1 mm) (Pb-free) | |
| | CY62167EV30LL-45BVI ^[31] | 51-85150 | 48-ball VFBGA (6 × 8 × 1 mm) | |

Ordering Code Definition



Note

31. This part can be operated in the V_{CC} range of 1.65 V to 2.25 V at 55 ns speed. It can also be operated in the V_{CC} range of 2.2 V–3.6 V at 45ns speed.

Package Diagrams

Figure 10. 48-Ball VFBGA (6 × 8 × 1 mm), 51-85150

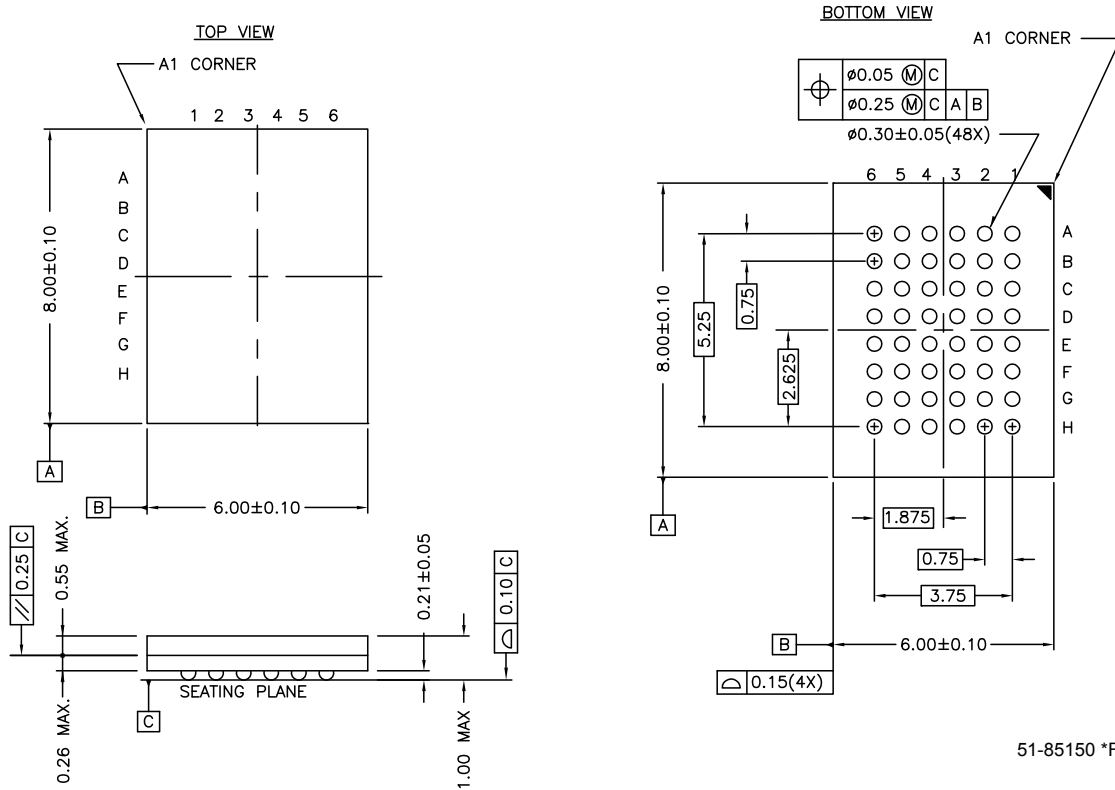
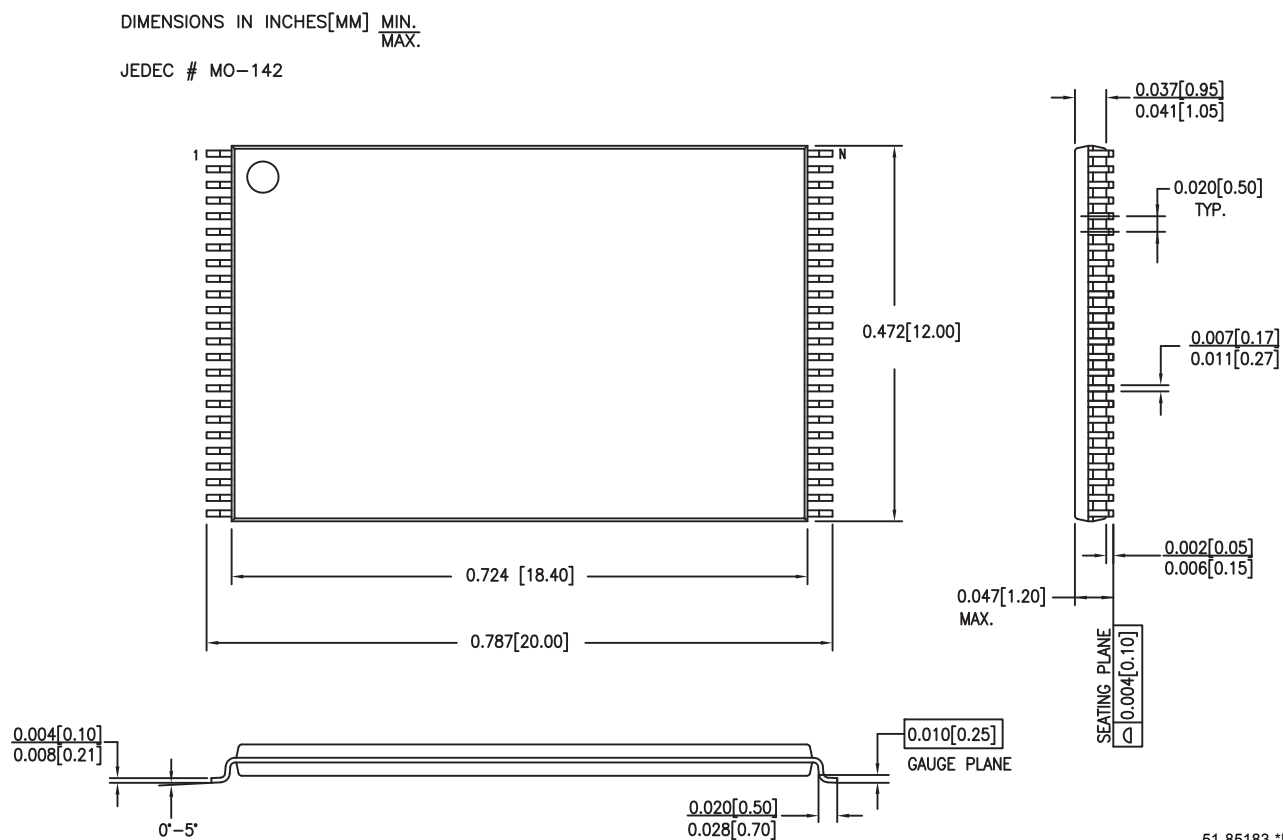


Figure 11. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



51-85183-B

Acronyms

| Acronym | Description |
|---------|---|
| BHE | byte high enable |
| BLE | byte low enable |
| CMOS | complementary metal oxide semiconductor |
| CE | chip enable |
| I/O | input/output |
| OE | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| VFBGA | very fine ball grid array |
| WE | write enable |

Document History Page

| Document Title: CY62167EV18 MoBL® 16 Mbit (1M x 16) Static RAM Document Number: 38-05447 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission date | Description of Change |
| ** | 202600 | AJU | 01/23/2004 | New Data Sheet |
| *A | 463674 | NXR | See ECN | Converted from Advance Information to Preliminary Changed $V_{CC(max)}$ from 2.20 V to 2.25 V Removed 'L' bin and 35 ns speed bin from product offering Changed ball E3 from DNU to NC Removed redundant foot note on DNU Changed the $I_{SB2(typ)}$ value from 1.3 μA to 1.5 μA Changed the $I_{CC(max)}$ value from 40 mA to 25 mA Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns Changed the I_{CCDR} Value from 8 μA to 5 μA Changed t_{OHA} , t_{LZCE} , t_{LZBE} , and t_{LZWE} from 6 ns to 10 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE} , t_{AW} , and t_{BW} from 40 ns to 35 ns Changed t_{PE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Updated 48 ball FBGA Package Information Updated the Ordering Information table |
| *B | 469182 | NSI | See ECN | Minor Change: Moved to external web |
| *C | 619122 | NXR | See ECN | Replaced 45 ns speed bin with 55 ns speed bin |
| *D | 1130323 | VKN | See ECN | Converted from preliminary to final Added footnote# 8 related I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 10 μA to 12 μA Changed I_{CCDR} spec from 8 μA to 10 μA Added footnote# 13 related AC timing parameters Changed t_{WC} spec from 45 ns to 55 ns Changed t_{SCE} , t_{AW} , t_{PWE} , t_{BW} spec from 35 ns to 40 ns Changed t_{HZWE} spec from 18 ns to 20 ns |
| *E | 1388287 | VKN | See ECN | Added 48-Ball VFBGA (6 x 7 x 1mm) package Added footnote# 1 related to FBGA package Updated Ordering Information table |
| *F | 1664843 | VKN/AESA | See ECN | Added CY62167EV30LL-45BVI part in the Ordering Information table Added footnote# 5 related to CY62167EV30LL-45BVI part |
| *G | 2675375 | VKN/PYRS | 03/17/2009 | Added CY62167EV18LL-55BVI part in the Ordering Information table |
| *H | 2904565 | AJU | 04/05/2010 | Removed inactive part from the ordering information table.Updated package diagrams. |
| *I | 2934396 | VKN | 06/03/10 | Added footnote #24 related to chip enable Updated template |
| *J | 3006301 | RAME | 08/12/2010 | Included BHE and BLE in I_{SB1} , I_{SB2} , and I_{CCDR} test conditions to reflect Byte power down feature. Removed 48-Ball VFBGA (6 x 7 x 1 mm) package related information. Added Acronyms and Ordering code definition. Format updates to match template. |
| *K | 3113908 | PRAS | 12/17/2010 | Updated Figure 1 and Package Diagram. |

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